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The origin of gate bias stress instability and hysteresis in monolayer WS_2 transistors

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ABSTRACT

Due to the ultra-thin nature and moderate carrier mobility, semiconducting two-dimensional (2D) materials have attracted extensive attention for next-generation electronics. However, the gate bias stress instability and hysteresis are always observed in these 2D materials-based transistors that significantly degrade their reliability for practical applications. Herein, the origin of gate bias stress instability and hysteresis for chemical vapor deposited monolayer WS_2 transistors are investigated carefully. The transistor performance is found to be strongly affected by the gate bias stress time, sweeping rate and range, and temperature. Based on the systematical study and complementary analysis, charge trapping is determined to be the major contribution for these observed phenomena. Importantly, due to these charge trapping effects, the channel current is observed to decrease with time; hence, a rate equation, considering the charge trapping and time decay effect of current, is proposed and developed to model the phenomena with excellent consistency with experimental data. All these results do not only indicate the validity of the charge trapping model, but also confirm the hysteresis being indeed caused by charge trapping. Evidently, this simple model provides a sufficient explanation for the charge trapping induced gate bias stress instability and hysteresis in monolayer WS_2 transistors, which can be also applicable to other kinds of transistors.

KEYWORDS

charge trapping, gate bias stress instability, hysteresis, WS_2, transistor

1 Introduction

In the past decades, silicon-based transistors have been the major workhorse for countless technological applications, such as integrated circuits, displays and many others. The characteristic length of silicon devices has then followed Moore's Law to scale below 5 nm in the current technology [1]; however, the continuous device down-scaling is extraordinarily challenging due to various issues, which include short channel effect, drain induced barrier lowering, etc. [2]. One proved solution is to utilize device channel materials with the atomic thickness in order to eliminate the adverse effect of device scaling [3]. In this case, since the surface states arising from dangling bonds of silicon channels are inevitable, drastically degrading the channels' carrier mobility and leading to the poor device performance, there is an urgent search for the alternative channel materials [4].

Fortunately, the advent of two-dimensional (2D) monolayer semiconductors, without any dangling bonds and surface states because of their van der Waals (VDW) interlayer interaction, may offer a perfect resolution to the problem here [5–7]. Even though the mechanical exfoliation of 2D materials can yield the perfect crystallinity of device channels, the required exfoliation processing schemes would significantly restrict their large-scale deployment [8–10]. Since then, extensive efforts have been invested to achieve bottom-up, wafer-scale and single-domain 2D monolayers with no defects for device fabrication [11–13]. In any case, owing to the complication of growth thermodynamics and kinetics, there are still surface defects existing in the VDW 2D materials [14, 15]. When they are configured into transistors, one direct consequence is the appearance of gate bias stress instability and hysteresis effect associated with their transfer characteristics, hindering their practical utilizations [16–18]. More importantly, these antagonistic effects would further interfere the precise determination of many device parameters that comprise of carrier mobility, threshold voltage, etc.

In this work, we investigate thoroughly the origin of gate bias stress instability and hysteresis effects observed in the chemical vapor deposited (CVD) monolayer WS_2 transistors. Due to the existence of defect trap charges, the device transfer characteristics (i.e. transfer curves) cannot be typically fitted by a linear relationship, which indicates the gate voltage dependent carrier mobility. Also, their device performances are strongly affected by the gate bias stress time, voltage sweeping rate and sweeping range, and temperature, all these

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influences are attributed to the charge trapping. Based on these charge trapping effects, a rate equation is then proposed to model the observed hysteresis phenomena with excellent consistency, designating the validity of the charge trapping model that the hysteresis is indeed caused by the charge trapping. All these results can not only provide a simple and effective model to describe the charge trapping induced gate bias stress instability and hysteresis effect in monolayer WS_2 transistors, but also deliver further insights to the charge trapping dynamics, potentially extendable to all other kinds of transistors.

2 Experimental

Monolayer WS_2 flakes were synthesized by a modified CVD using the growth promoter of NaOH as previously reported [19]. The degenerately p-doped Si with a thermally grown oxide layer (270 nm thickness) was employed as the substrate. After the growth, global back-gate field-effect transistors (FETs) were then fabricated on the processed substrate. Ultraviolet (UV) lithography was used to pattern the source/drain regions, followed by the electron-beam deposition of Ti/Au (5 nm/80 nm) electrodes and lift-off process. All electrical measurements were carried out in a vacuum probe station. Agilent 1500B semiconductor analyzer was utilized to measure the electrical properties of fabricated transistors. During the measurement, the probe station is pumped down to a vacuum level of less than 2×10^{-4} Pa.

3 Results and discussion

In order to initiate this study, the global back-gate FETs were first configured utilizing the synthesized monolayer WS_2, where the typical grain size was about 100 μm for these monolayers. The optical microscope image of the fabricated device is then shown in the inset of Fig. 1(a), while the profile of one typical monolayer WS_2 sheet is labeled by the orange-colored line. The structure of the back-gate FET is shown in the inset of Fig. 1(b). Based on the output and transfer characteristics, the device exhibits a distinctive n-type conductivity (Figs. 1(a) and 1(b)). The almost linear relationship between the source-drain current (I_{ds}) and source-drain voltage (V_{ds}) indicates the ohmic-like contact between WS_2 and electrodes (Fig. 1(a)). Also, the ON/OFF current ratio can be directly obtained from the logarithmic plot of the transfer curve (Fig. 1(c)), in which the ratio is found to be 10^7 with a sub-threshold swing (SS) of 6.2 V·dec^{-1}. The large SS suggests the competitive of other capacitances with gate capacitance, such as depletion capacitance and defects related capacitance [20]. The depletion capacitance here should be small due to the ultrathin thickness of the monolayer WS_2 [21]. This way, defects related capacitance should have significant contributions to the large SS, indicating a large amount of defects in the SiO_2–WS_2 interface or below WS_2. For a source-drain voltage of 50 mV, the linear region of the transfer characteristics can be described by the following equation

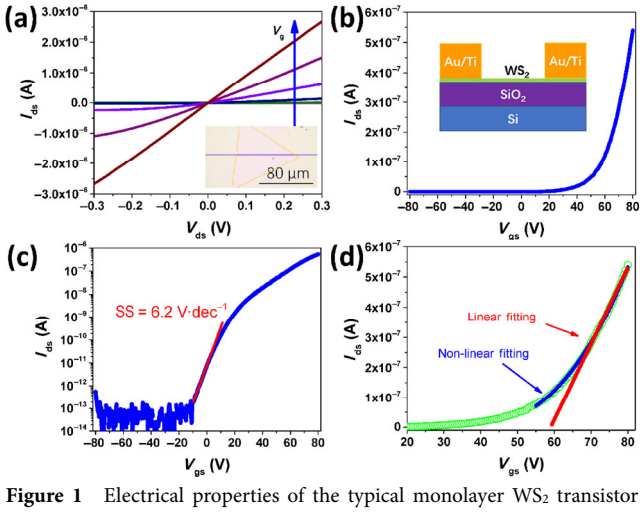

Figure 1 Electrical properties of the typical monolayer WS_2 transistor measured at room temperature under vacuum. (a) Output characteristics with the gate voltage varied from −80 to 80 V with a step of 20 V. Inset shows the optical microscope image of the measured device. (b) Transfer characteristics with the source-drain voltage of 50 mV and sweeping rate of 3.8 V·s^{-1}. Inset shows the schematic of the transistor (not drawn in scale). (c) Logarithmic plot of the device transfer curve presented in (b). (d) Linear and non-linear fittings of the transfer curve presented in (b).

$$I_{ds} = \mu C_{ox} \frac{W}{L}(V_{gs} - V_T)V_{ds} \quad (1)$$

where μ is the field-effect electron mobility, C_{ox} is the gate capacitance per unit area (1.28×10^{-4} F·m^{-2} for 270-nm-thick SiO_2), L is the channel length (2 μm), W is the channel width (86 μm) and V_T is the threshold voltage. By fitting the curve using Eq. (1), the field-effect electron mobility is calculated to be 0.92 cm^2·V^{-1}·s^{-1} with the threshold voltage of 59.1 V. However, it is evident that the fitting is valid only for the large gate bias, suggesting that the electron mobility may also be dependent on the applied gate voltage (Fig. 1(d)). In fact, this gate-dependent mobility has been observed in monolayer MoS_2 and organic thin-film transistors [16, 22]. Technically, there are several contributions to the gate-dependent electron mobility. The first one can be associated to the reduced Coulombic scattering of charge carriers propagating in the device channel [23, 24]. When a relatively high gate voltage is applied, a high electron density can be induced to enhance the screening of Coulombic scattering potential, leading to improved electron mobility at high gate voltage. The second contribution can be related to the existence of defect trap charges in the device channel [16, 24]. In this case, the electron transport is limited by the charge traps localized near the conduction band edge of WS_2. To be specific, the Fermi level at the insulator–semiconductor interface would move towards the band edge once a positive gate voltage is applied, leading to the trap filling. As a result, charge trapping becomes less efficient such that the electron mobility gets increased accordingly. Here, the contribution of defect trap charges is more plausible because CVD synthesized WS_2 monolayers usually have a significant number of defects, acting as electron traps [25–28]. The charge traps near the SiO_2–WS_2 may also affect the transport properties as well [29, 30]. At the same time, the gate-dependent carrier mobility can also be modeled by the following semi-empirical relationship [22]

$$\mu = \kappa(V_{gs} - V_T)^{\alpha} \quad (2)$$

where κ and α are the fitting parameters, and V_T is the threshold voltage. By substituting Eq. (2) into Eq. (1), there would be a non-linear relationship resulted to describe the device transfer characteristics as below

$$I_{ds} = \frac{W}{L} C_{ox} \kappa (V_{gs} - V_T)^{1+\alpha} V_{ds} \quad (3)$$

Surprisingly, as demonstrated in Fig. 1(d), the transfer curve can be well fitted by using Eq. (3). From the curve fitting, the threshold voltage, parameters of κ and α are found to be 26.7 V, 6.7×10^{-5} cm^2·V$^{-(1+\alpha)}$·s^{-1} and 2.16, respectively. The electron mobility can then be estimated as 0.36 cm^2·V^{-1}·s^{-1} for the V_{gs} of 80 V, which is smaller than that obtained from the linear fitting. The relatively large value of the α parameter indicates the strong dependence

of mobility on the gate bias, suggesting the presence of large amounts of electron traps in the monolayer WS_2 here.

Considering the existence of electron traps, it is necessary to investigate the effect of gate bias stress on the transport properties of monolayer WS_2 transistors. In particular, the device transfer curves sweeping from −80 to 80 V under different negative gate bias stress times as well as sweeping from 80 to −80 V under different positive gate bias stress times were measured. For the positive (negative) gate bias stress, a constant gate voltage of 80 V (−80 V) was first applied for a specific time before measuring the transfer curve. During the measurement, it is also noted that once the device got recovered to its initial state, there would be an idle time of 30 min for the execution of next measurement with different stress times to ensure the return of device equilibrium state for the consistent comparison among all the data collected. As depicted in Fig. 2(a), the transfer curve gradually shifts to the positive direction for the increasing positive gate bias stress times. Since the transfer curves were not well fitted in a linear manner (Fig. 1(d)), the exact value of threshold voltage can only be obtained from the non-liner fitting using Eq. (3). For simplicity, the maximum output current (I_{ds}) under different stress times are also used

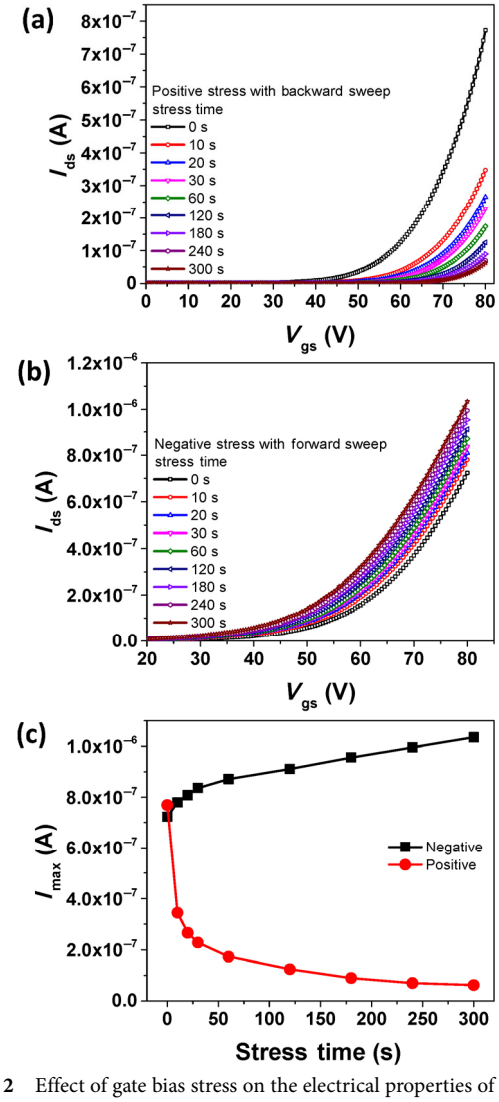

Figure 2 Effect of gate bias stress on the electrical properties of a monolayer WS_2 transistor. (a) Positive stress under different stress time. (b) Negative stress under different stress times. (c) Maximum output current (I_{max}) as a function of stress time. During the measurement of these transfer curves under vacuum, the source-drain voltage is fixed at 50 mV, while the voltage sweeping rate is controlled to 7.6 V·s^{-1}.

to illustrate the effect of gate bias stress on the electrical properties of monolayer WS_2 transistors. It is observed that the current drops quickly for the stress time of first 30 s and then slowly down to a saturated value (Fig. 2(c)). On the other hand, the transfer curve shifts to the negative direction for the increasing negative gate bias stress times (Fig. 2(b)). The maximum output current is found to increase gradually with the increasing stress time and then reaches a steady-state value, where all these observations are contrary to the ones under positive stress (Fig. 2(c)).

Actually, this gate bias stress effect has been observed in 2D materials-based transistors, such as MoS_2 and InSe, in which majority of research teams attribute this effect arising from water/oxygen adsorption and desorption processes [31, 32]. However, the influence coming from gas molecules is minimized in the current investigation because all the electrical measurements were carried out under vacuum. As a result, the existence of intrinsic or interface defects of the monolayer WS_2 would be the reason for the observation of gate bias stress effect, where these defects contribute to the electron traps. In explicit, when the defect-related traps have a density of N_t, a portion of these traps, such as n_{t0}, are occupied by electrons at the gate voltage of 0 V (V_{gs} = 0 V = V_{g0}). For the positive gate bias stress, the number of electrons trapped in these defects at V_{g0} would increase to n_{tp} such that $n_{tp} > n_{t0}$. For the negative gate bias stress, there are less electrons trapped in the defects, labeled as n_{tn}, as compared to the ones at V_{g0}, and hence $n_{tn} < n_{t0}$. Simultaneously, n_0, n_p, and n_n can represent the free electron density at V_{g0} without gate bias stress, under positive gate bias stress and negative gate bias stress, respectively. The amount of total charge induced by the gate bias can be denoted by N at V_{g0}. This way, $N = n_0 + n_{t0} = n_p + n_{tp} = n_n + n_{tn}$, which leads to the relationship of $n_p < n_0 < n_n$. If the electron density is assumed to be the dominant factor in this analysis, the observed gate bias stress instability (i.e. significant output current variation under different gate bias stress conditions) can be well explained by the electron trapping mechanism. As the gate bias stress time is long enough, most of the traps are fully occupied (empty) for the positive (negative) gate bias stress. The density of free electrons would then keep almost constant, leading to the insignificant change of current under a long bias stress time. It is also worth mentioning that the maximum currents with bias time of 0 s are different for the negative and positive gate bias stress, which is attributed to the different sweeping direction. The sweeping would act as the equivalent gate bias, leading to the different maximum currents.

In principle, the existence of traps in the device channel would lead to both gate bias stress instability as well as hysteresis effect for transistors [33, 34]; therefore, it is important to evaluate the hysteresis behavior of monolayer WS_2 transistors. Specifically, the double sweep transfer curves (starting from −80 to 80 V and then 80 to −80 V) with different sweeping rates are displayed in Fig. 3(a), where obvious hysteresis effects are observed. In order to characterize the magnitude of hysteresis, the threshold voltage difference between forward and backward sweeps is extracted according to Eq. (3) and compiled in Fig. 3(b). It is apparent that the hysteresis increases with the decreasing sweep rates. The maximum output current at V_g = 80 V is also reduced with the decreasing sweeping rates as given in Fig. 3(d). For the forward sweep, the negative sweeping range (−80 to 0 V) provides a negative gate bias stress, leading to the increase of output current. Once the positive sweeping range (0 to 80 V) is implemented, a positive gate bias stress is resulted causing the decrease of current of the backward sweep. As a result, a hysteresis is observed for the double sweep transfer curves. The change in the sweeping rate is equivalent to the alteration

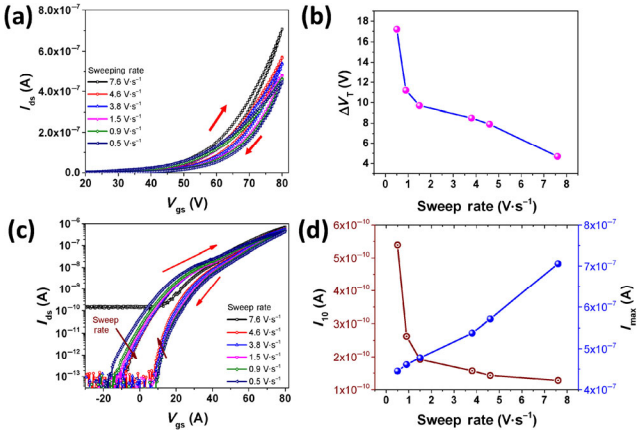

Figure 3 Detailed transfer characteristics of a typical monolayer WS_2 transistor. (a) Double sweep transfer curves with different sweeping rates. (b) Change of threshold voltage as a function of the voltage sweeping rate. (c) Logarithmic plot of the double sweep transfer curves presented in (a). The red-colored arrows indicate the voltage sweeping direction, while the brown-colored arrows designate the increasing sweeping rate for different curves. (d) Forward-sweeping current (I_{10}) at V_{gs} =10 V and I_{max} as a function of the voltage sweeping rate.

of the gate bias stress time. For a slow sweeping rate, the negative gate bias stress time is sufficiently long, leading to the increase of output current. However, when the gate sweeping enters the positive range, the positive gate bias stress begins and induces the decrease of output current. In this regard, during the forward sweep, the output current at a small positive gate voltage with a slow sweeping rate should have a larger magnitude than that with a fast sweeping rate. Similarly, the output current at a large positive gate voltage with a slow sweeping rate should have a smaller magnitude than that with a fast sweeping rate. This phenomenon can be clearly witnessed from the logarithmic plot of the transfer curves as shown in Fig. 3(c). To further demonstrate this phenomenon clearly, the forward sweeping current at V_{gs} = 10 V as a function of the sweeping rate is presented in Fig. 3(d). Remarkably, the current decreases with the increasing sweeping rates, while the current at V_{gs} = 80 V (i.e. the maximum ON-state current) increases with the increasing sweeping rate, being consistent with the discussion above. For the backward sweep, the positive gate bias stress is maintained in the positive range (80 to 0 V), which gives to the continuous decreasing trend of the current. Consequently, the current with a slow sweeping rate is still smaller in the magnitude as compared with that with the fast sweeping rate (Fig. 3(c)). In this case, it is evident that the hysteresis is enlarged when a slow sweeping rate is applied. Notably, when the device is measured with the fastest sweeping rate, it seems to give the highest OFF-state current for the backward sweep. This high OFF-state current may not be an accurate representation of the device response, which can be attributed to the small integration time during measurement.

To further shed light onto the hysteresis behavior of monolayer WS_2 transistors, the double sweep transfer curves with different gate sweeping ranges were evaluated and illustrated in Fig. 4. The forward sweeping transfer curves are found to almost coincide with each other, suggesting that the variation of sweeping range has little influence on the ON-state current for the forward sweep, while the influence of sweep ranging is relatively large on the backward sweeping curves (Fig. 4(a)). Moreover, the currents in the sub-threshold region of both forward and backward sweeps are also observed to be strongly affected by the sweeping range (Fig. 4(b)). Based on the threshold voltage difference between forward and backward sweeps, it is obvious that the threshold voltage difference increases with the

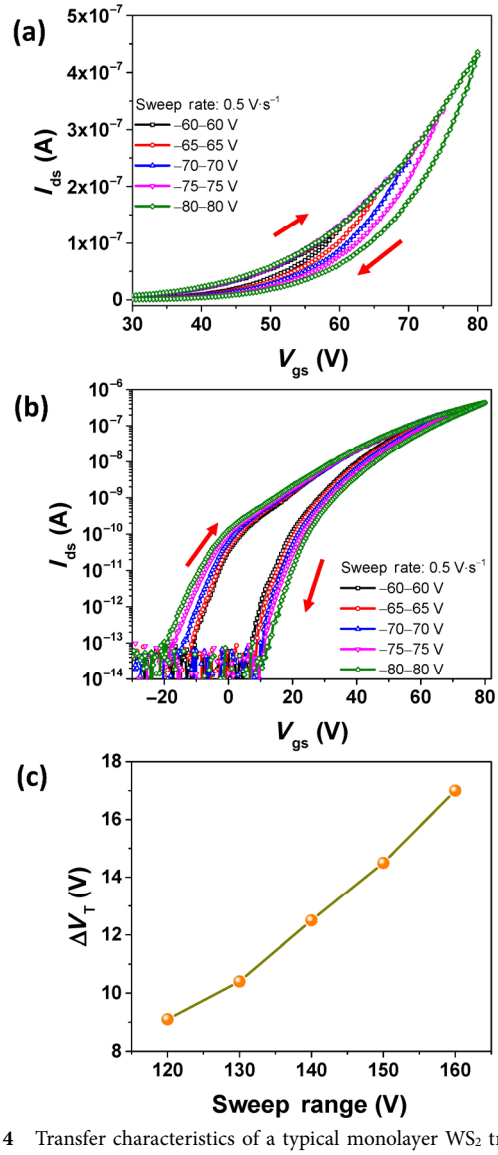

Figure 4 Transfer characteristics of a typical monolayer WS_2 transistor with different gate sweeping ranges. (a) Linear plot. (b) Logarithmic plot. (c) Threshold voltage difference as a function of the sweeping range. The source-drain voltage is 50 mV while the sweeping rate is 0.5 V·s^{-1} for all the measurement.

increasing sweeping ranges (Fig. 4(c)). In other words, the hysteresis would increase with the increasing sweeping range. Technically, the current in the sub-threshold region is controlled by carrier diffusion, which is highly sensitive to the change of free carriers in the channel such that a little change in the carrier density would result in a much larger change in current. For the forward sweep with a large sweeping range, the negative gate bias stress is stronger, which leads to a larger free carrier density in the sub-threshold region. Therefore, the sub-threshold current with a larger sweeping range would be enhanced for the forward sweep. Since a relatively slow sweeping rate of 0.5 V·s^{-1} is used, the trapping of carriers tends to be stable, leading to little change of the ON-state current. Likewise, for the backward sweep with a large sweeping range, the positive gate bias stress time is increased, which leads to a faster current drop. As a result, the hysteresis is enlarged for the larger sweeping range.

Because charge trapping and de-trapping are thermodynamic processes that are sensitive to temperature. In this investigation, the temperature dependent hysteresis curves were as well measured and shown in Fig. 5. It can be seen that the hysteresis of transfer curves becomes enlarged at high temperature (Fig. 5(a)).

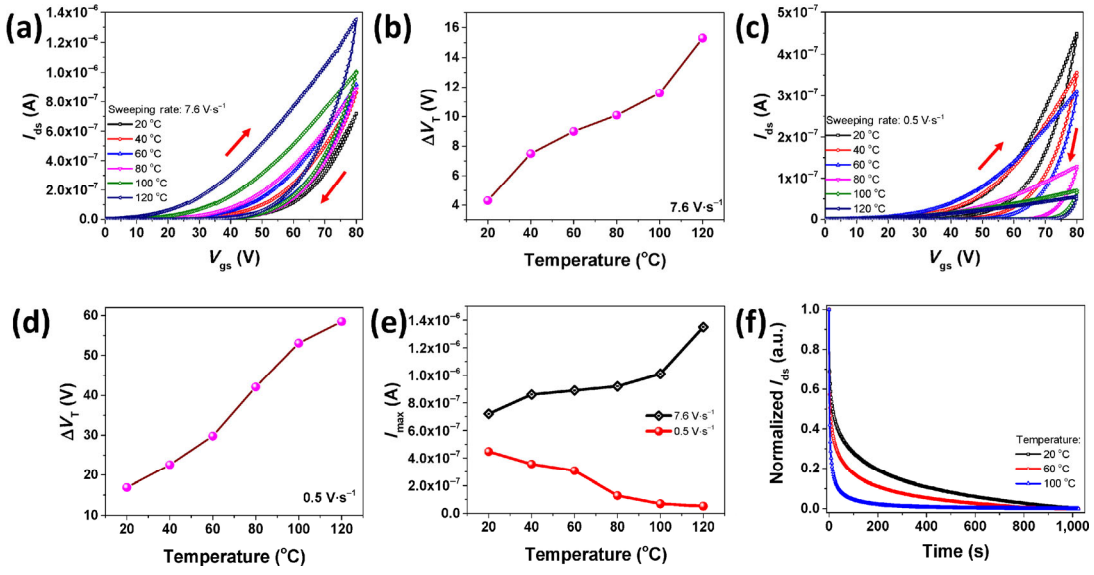

Figure 5 Temperature dependent electrical behaviors of a typical monolayer WS_2 transistor. (a) Transfer curves with a sweeping rate of 7.6 V·s^{-1}. (b) Threshold voltage difference as a function of temperature for the transfer curves measured with a sweeping rate of 7.6 V·s^{-1}. (c) Transfer curves with a sweeping rate of 0.5 V·s^{-1}. (d) Threshold voltage difference as a function of temperature for the transfer curves measured with a sweeping rate of 0.5 V·s^{-1}. (e) Maximum output current as a function of temperature measured at different sweeping rates. (f) Normalized output currents (at V_g = 80 V) as a function of trap lifetime measured at different temperatures. The source-drain voltage is 50 mV for all the measurement.

The extracted threshold voltage difference between forward and backward sweeps is also found to increase with the increasing temperatures (Fig. 5(b)), which further indicates the enlarged hysteresis here. In addition, the maximum output current increases when the temperature elevates (Fig. 5(e)). With a relatively slow sweeping rate of 0.5 V·s^{-1}, the hysteresis increases with the increasing temperatures (Figs. 5(c) and 5(d)); nevertheless, the maximum output current decreases accordingly (Fig. 5(e)). For semiconductors, the conductivity increases with temperature due to the thermally induced charge carriers at high temperatures. It is anticipated to have the enhanced current at high temperatures, being similar to the case of fast sweeping. In contrast, the reduced current at high temperatures for slow sweeping can be attributed to the existence of charge traps. The trapping of electrons is usually described by the capture rate of R, which is analytically expressed as [35]

$$R = Svn(N_t - n_t) \quad (4)$$

where S is the capture cross-section, v is the thermal velocity, n is the free carrier density and n_t is the traped electron density. The capture cross-section of S is a trap-related parameter, associated with the intrinsic properties of the traps. The thermal velocity of v have to satisfy the relationship of $mv^2/2 = k_BT$, where m is the mass of corresponding carriers, k_B is the Boltzmann constant and T is the temperature in Kelvin. This way, R must increase with temperature. In this case, the free carrier density would reduce at a faster rate at high temperatures as compared to that at low temperatures. If the sweeping rate is slow, most of the gate induced free electrons are captured by traps, leading to a reduced current. To confirm the increased charge trapping rate at high temperature, the transient current curves were measured at V_g = 80 V as shown in Fig. 5(f). Based on the normalized transient current curves, it is observed that the current drops at a faster rate at high temperatures, which is consistent with the data trend of the increased capture rate. Considering the free electrons have a lifetime of τ, τ can be described as

$$\tau = 1/\, Sv(N_t - n_t) \quad (5)$$

According to Eq. (5), the lifetime decreases with the increasing temperature. Also, the transient current curves reveal the changes of lifetime with temperature. Notably, these curves cannot be well fitted by a single exponential function, indicating the presence of multi-kinds of traps in the monolayer WS_2 channel. The average lifetimes at different temperatures can be obtained by extracting the time at 1/e, which correspond to 48.1, 15.7, and 3.2 s at 20, 60, and 100 °C, respectively (Fig. 5(f)). Obviously, the determined lifetime decreases with the increasing temperatures, being consistent with Eq. (5). The reduced lifetime also leads to the enlarged hysteresis, which will be discussed in detail in the subsequent section.

At the same time, it is important to illustrate the relationship between gate sweeping rate and carrier lifetime for the transfer characteristics of monolayer WS_2 transistors. In this work, a rate equation is proposed with the consideration of only n-type semiconductor-based devices for simplicity. Generally, when an n-type transistor is operated in its ON-state, the free carrier density of n would satisfy a rate equation of

$$\frac{dn}{dt} = -\frac{n}{\tau} + \gamma v_s \quad (6)$$

where v_s is the sweeping rate during the measurement of transfer curves and t is the time. The parameter of γ can then be calculated by the expression of $\gamma = C_{ox}/dq$, in which C_{ox}, d and q represent the unit area capacitance, thickness of the channel, and elemental charge value, respectively. With the above rate equation as well as the threshold voltage being zero for the forward sweep, the channel current can be described as the following (with detailed discussion given in the Electronic Supplementary Material (ESM))

Forward sweep: $$I_{ds} = b\kappa\gamma\tau v_s^{\alpha+1} t^{\alpha}\left(1 - e^{-\frac{t}{\tau}}\right) \quad (7a)$$

Backward sweep:

$$I_{ds} = b\kappa(V_{gs\_max} + v_s t - V_T)^{\alpha}\left[\gamma v_s \tau + (n_0 - \gamma v_s \tau)e^{-\frac{t}{\tau}}\right] \quad (7b)$$

where $b = qAE$, q is the elemental charge value, A is the cross section area of the channel, E is the electric field between source and drain electrodes, V_{gs_max} is the maximum gate

voltage during the forward sweep, V_T is the gate voltage for which the carrier density is zero during the backward sweep. It should be also noted that the parameters of κ, α and τ for the backward sweep should be different from the ones of forward sweep, or else the current at V_{gs_max} is different, which would be contradictory to the experimental results here. One possible origin is caused by the finite threshold voltage for the backward sweep. In fact, the filling levels of traps are different for both forward and backward sweeps, where the average values of κ, α, and τ would be altered for these two different kinds of sweeps. In this work, the value of κ is tuned to make the output current matching the one at V_{gs_max} in the following discussion. According to Eq. (7), finite τ and v_s would lead to the significant hysteresis. For simplicity, the device response near the sub-threshold region is not considered, especially when the behavior near the sub-threshold region cannot be reliably reproduced.

After that, the effect of different power coefficient values of α on the device transfer characteristics is also discussed. As shown in Fig. 6(a), there is not any hysteresis for the carriers with infinite lifetime. In other words, if there are no charge traps existed in the device channel, there would not be any hysteresis. Once the α value increases from 0 to 2, the corresponding transfer curve would change from linear to super-linear, being consistent with the experimental results. The hysteresis effect starts to appear when the carriers have a finite lifetime as depicted in Fig. 6(b). For $\alpha = 0$, the forward sweeping curve is sub-linear, while the backward sweeping one is super-linear. Furthermore, the maximum output current decreases as compared with the one without hysteresis. In fact, the condition of $\alpha = 0$ corresponds to the constant carrier mobility, which is the ideal case for transistors. In reality, the carrier mobility is not a constant but a function of V_{gs}. Hence, α is always bigger than zero. For the case of monolayer WS_2 transistors, the α value is found to be close to 2 based on the curve fitting. The condition of $\alpha = 2$ would then be applied to the subsequent discussion. In this case, both forward and backward sweeping curves are super-linear, being well consistent with the experimental results (Fig. 6(b)); however, they have a lower current density as compared with the ones without hysteresis.

Once the condition of $\alpha = 2$ is fixed, the device transfer characteristics were simulated with different parameters. As given in Fig. 7(a), the hysteresis decreases with the increasing sweeping rate, while the output current approaches the curve without hysteresis for the fast sweeping rate, being consistent with the results shown in Fig. 3(a). These results also suggest that a fast sweeping rate is needed to obtain the accurate assessment of device parameters. The transfer curves with different sweeping ranges are then depicted in Fig. 7(b), which agrees well with the experimental findings illustrated in Fig. 4(a). Importantly, as displayed in Fig. 7(c), when the lifetime of free carriers increases, the hysteresis reduces and the current

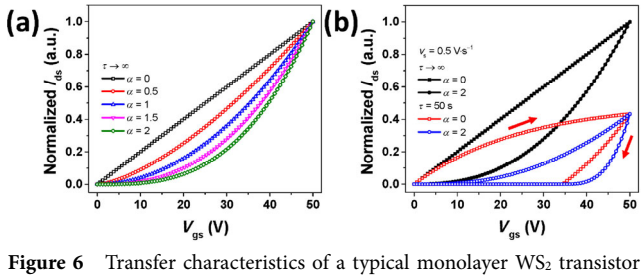

Figure 6 Transfer characteristics of a typical monolayer WS_2 transistor simulated with different α values. (a) The carrier lifetime is infinite. The current is normalized to the maximum output current of each curve. (b) The carrier lifetime is set at 40 s with a sweeping rate of 0.5 V·s^{-1}. The current is normalized to the maximum output current of each α for τ approaching ∞.

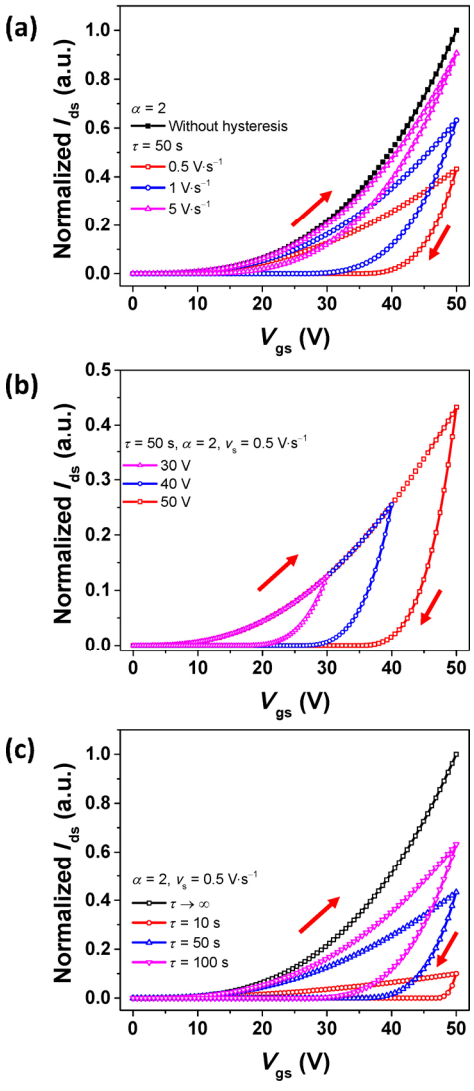

Figure 7 Transfer characteristics of a typical monolayer WS_2 transistor simulated with $\alpha = 2$ under different conditions. (a) Different sweeping rate. (b) Different sweeping range. (c) Different carrier lifetime. All curves are normalized to the curves without hysteresis.

increases. The reduced hysteresis with increased carrier lifetime is consistent with the temperature dependent transfer curves (Figs. 5(a) and 5(c)). All these observations indicate that the simple assumption of carrier trapping can account for most of the hysteresis phenomenon, validating the trapping model. It should also be noticed that no gate bias stress and sub-threshold effects are considered in the derivation of Eq. (7); therefore, the gate bias stress effect and sub-threshold behavior of transistors do not aim to be reproduced here. Moreover, the lifetime of free carriers may not be a constant value according to Eq. (5), which makes the situation more complicated in real cases, with further investigation required.

Due to the appearance of hysteresis, the channel current cannot be well fitted by Eq. (3), especially since this equation does not consider the decay of current with time. As our model developed here considers the time decay effect of the output current, it would provide a more accurate fitting to the experimental data. In this regard, we utilize Eq. (7) to fit all the obtained experimental curves. For example, fittings were made for the forward sweeps in order to obtain the parameters of Eq. (7). If the average lifetime during the sweeps is assumed to be 48 s as obtained from the I–t curve, only the fastest sweeping curve exhibits the perfect match with experimental findings as presented in Fig. 8(a) and Fig. S1 in the

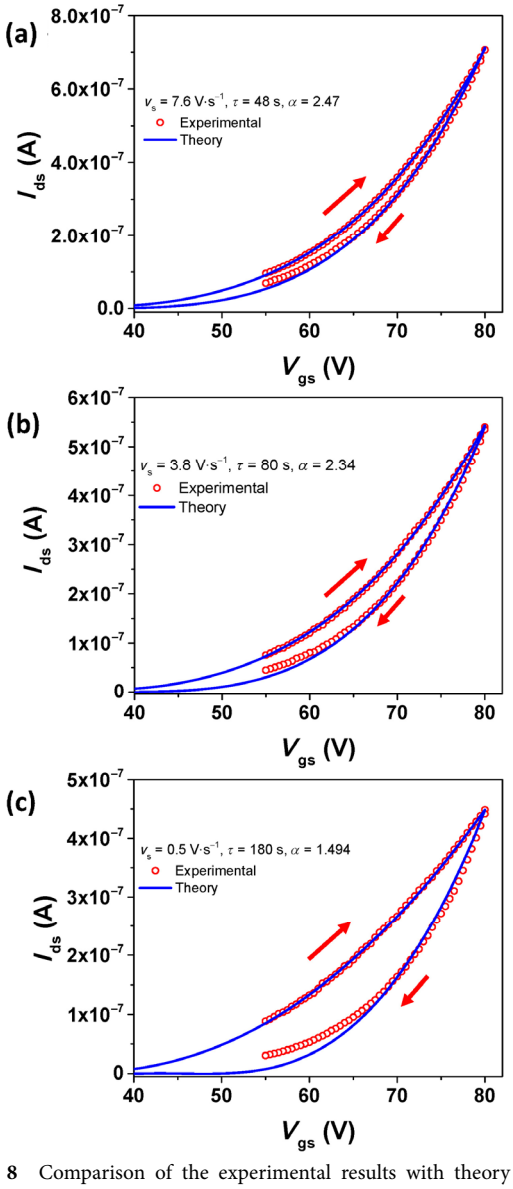

Figure 8 Comparison of the experimental results with theory under different sweeping rate: (a) 7.6 V·s^{-1}, (b) 3.8 V·s^{-1}, and (c) 0.5 V·s^{-1}.

ESM. The theoretical prediction deviates seriously for the slowest sweeping curve (Fig. S1(c) in the ESM). Based on Eq. (5), the carrier lifetime increases with the deceasing empty trap centers. For the slow sweeping rate, the filling levels of traps are larger than those with a fast sweeping rate, which leads to a larger value of the average carrier lifetime. By tuning the average carrier lifetime in Eq. (7), the experimental results can be well fitted (Fig. 8). The deviation at small current levels may be caused by sub-threshold effect or other defects. In any case, the power coefficient of α decreases with the increasing average carrier lifetime, which can be explained by the reduced dependence of carrier mobility with gate voltage due to the increased filling levels of charge traps for the slow sweeping rate. Actually, the appearance of gate bias stress effect and hysteresis of FETs is detrimental to most of the applications; therefore, it is essential to minimize these adverse effects. Since the gate bias stress effect and hysteresis are originated from the charge traps existing in the device channels, one effective solution is to reduce these charge traps by using high-quality 2D WS_2 channels, repairing defects in these channels or integrating with high-quality dielectric materials (e.g. BN) as surface passivation. This way, the instability and hysteresis issues of these 2D WS_2-based FETs can be alleviated.

4 Conclusion

In summary, we have systematically studied the gate bias stress instability and hysteresis effect in monolayer WS_2 transistors. It is found that the transfer characteristics of monolayer WS_2 transistors cannot be modelled by the conventional linear relationship, while the carrier mobility satisfies the power law relationship with gate voltage, indicating the existence of charge traps. In addition, the transistors show the strong gate bias effect such that the channel current decreases (increases) for the positive (negative) gate bias stress. This stress effect would be further enhanced when a longer gate bias stress time is applied. The transistors also exhibit significant hysteresis with the double gate sweeps. This hysteresis is observed to increase with the decreasing sweeping rate, increasing sweeping range and increasing temperature. Apart from hysteresis, the output current would decrease with time and even at a much faster rate at high temperature, attributable to the fast capture of free carriers. Based on experimental results, a rate equation considering the trapping of free carriers is then proposed and developed to explain the observed phenomena. Perfect consistency is observed between experimental data and theoretical prediction, which suggest the validity of the model and further indicate the hysteresis being indeed caused by charge trapping. All these results can evidently provide a simple model for the analysis of gate bias stress instability and hysteresis effect encountered in transistors.

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